Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims for this application.

1. (Currently Amended) A dynamic CMOS level shifter circuit apparatus in a digital electronic system for shifting a signal of a first logic family at a first lower voltage level to a second higher voltage level for a second logic family, said shifter circuit apparatus being connected between a power supply terminal and a ground terminal and comprising:

a first transistor pair comprising a first PMOS and a first NMOS transistor connected in series;

a second transistor pair comprising a second PMOS and a second NMOS transistor connected in series;

a power-down control PMOS transistor; and

means for supplying a power-down control signal to the gate of the power-down control PMOS transistor, the power-down control signal being changed to a high state for a predetermined period of time when the signal from the first logic family changes state; wherein:

said first and second transistor pairs are connected in parallel, and said parallel connection is connected in series with said power-down control PMOS transistor across ~~the power and ground levels of said system~~ the power supply terminal and the ground terminal, wherein said control PMOS transistor is connected at the power supply terminal~~end~~, and said first and second NMOS transistors at the ground terminal~~end~~;

the node at which the drain terminals of said transistors of said first transistor pair being connected together is also connected to the gate of said second PMOS transistor, and the node at which the drain terminals of said transistors of said second transistor pair being connected together is also connected to the gate of said first PMOS transistor; and

the gate terminal of said first NMOS transistor serves as a ~~the~~ signal input for receiving the signal from said first ~~input~~ logic family; the gate terminal of said first PMOS transistor serves as the shifted output of said shifter circuit apparatus; and the power-down control signal controls the gate terminal of said power-down control PMOS transistor ~~is controlled by a power down control signal~~ to cut off the power to said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition.

2. (Currently Amended) The shifter circuit apparatus of claim 1, further comprising a first inverter and a second inverter, wherein said first and second inverters are connected in series, the input of said first inverter is connected to said shifted output, wherein ~~and~~ the output of said first inverter generates a voltage complementary to the voltage output by said shifted output, and the output of said second inverter generates a voltage same as the voltage ~~complementary pair~~ output by ~~of~~ said shifted output.

3. (Currently Amended) A dynamic CMOS level shifter circuit apparatus in a digital electronic system for shifting a signal of a first logic family at a first lower voltage level to a second higher voltage level for a second logic family, said shifter circuit apparatus being connected between a power supply terminal and a ground terminal and comprising:

a first transistor pair comprising a first PMOS and a first NMOS transistor connected

in series;

a second transistor pair comprising a second PMOS and a second NMOS transistor connected in series;

a power-down control PMOS transistor;

a first inverter and a second inverter; and

means for supplying a power-down control signal to the gate of the power-down control PMOS transistor, the power-down control signal being changed to a high state for a predetermined period of time when the signal from the first logic family changes state; wherein:

said first and second transistor pairs are connected in parallel, and said parallel connection is connected in series with said power-down control PMOS transistor across the power supply terminal and ground terminal~~levels of said system~~, wherein said control PMOS transistor is connected at the power supply terminal ~~end~~, and said first and second NMOS transistors at the ground terminal ~~end~~;

the node at which the drain terminals of said transistors of said first transistor pair being connected together is also connected to the gate of said second PMOS transistor, and the node at which the drain terminals of said transistors of said second transistor pair being connected together is also connected to the gate of said first PMOS transistor; and

the gate terminal of said first NMOS transistor serves as a ~~the~~ signal input for receiving the signal from said first ~~input~~ logic family; the gate terminal of said first PMOS transistor is connected to the input of said first inverter; the output of said first inverter is connected to the input of said second inverter; the output of said second inverter generating a voltage same ~~serves~~ as the voltage output by said shifted output of said shifter circuit apparatus; and the power-down control signal controls the gate terminal of said power-down control PMOS

transistor ~~is controlled by a power down control signal~~ to cut off the power to said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition.

4. (Currently Amended) The shifter circuit apparatus of claim 3, further comprising a third N~~P~~MOS transistor, wherein the drain and source terminals of said third NMOS transistor are connected respectively to the input of said first inverter and the ground terminal ~~of said system~~.

5. (Currently Amended) The shifter circuit apparatus of claim 3, further comprising a resistor connected across the input of said first inverter and the ground terminal ~~of said system~~.

6. (Currently Amended) A dynamic CMOS level shifter circuit apparatus in a digital electronic system for shifting a signal of a first logic family at a first lower voltage level to a second higher voltage level for a second logic family, said shifter circuit apparatus being connected between a power supply terminal and a ground terminal and comprising:

a first transistor pair comprising a first PMOS and a first NMOS transistor connected in series;

a second transistor pair comprising a second PMOS and a second NMOS transistor connected in series;

a power-down control PMOS transistor;

a first inverter and a second inverter;

a third NMOS transistor; and

means for supplying a power-down control signal to the gate of the power-down control PMOS transistor, the power-down control signal being changed to a high state for a predetermined period of time when the signal from the first logic family changes state; wherein:

said first and second transistor pairs are connected in parallel, and said parallel connection is connected in series with said power-down control PMOS transistor across the power supply terminal and ground terminal ~~levels of said system~~, wherein said control PMOS transistor is connected at the power supply terminal~~end~~, and said first and second NMOS transistors at the ground terminal~~end~~;

the node at which the drain terminals of said transistors of said first transistor pair being connected together is also connected to the gate of said second PMOS transistor, and the node at which the drain terminals of said transistors of said second transistor pair being connected together is also connected to the gate of said first PMOS transistor; and

the gate terminal of said first NMOS transistor serves as a ~~the~~ signal input for receiving the signal from said first ~~input~~ logic family; the gate terminal of said first PMOS transistor is connected to the input of said first inverter; the output of said first inverter is connected to the input of said second inverter; and the output of said second inverter generates a voltage same ~~serves~~ as the voltage output by the shifted output of said shifter circuit apparatus; the drain and source terminals of said third NMOS transistor are connected respectively to the input of said first inverter and the power-down control signal controls the gate terminal of said power-down control PMOS transistor ~~is controlled by a power-down control signal~~ to cut off the power to said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition.

7. (Currently Amended) The shifter circuit apparatus of claim 1, further comprising a third PMOS transistor connected between the power supply terminal ~~level of said system~~ and said power-down control PMOS transistor.

8. (Currently Amended) A dynamic CMOS level shifter circuit apparatus in a digital electronic system for shifting a signal of a first logic family at a first lower voltage level to a second higher voltage level for a second logic family, said shifter circuit apparatus being connected between a power supply terminal and a ground terminal and comprising:

a first transistor pair comprising a first PMOS and a first NMOS transistor connected in series;

a second transistor pair comprising a second PMOS and a second NMOS transistor connected in series;

a third PMOS transistor;

a power-down control PMOS transistor; and

means for supplying a power-down control signal to the gate of the power-down control PMOS transistor, the power-down control signal being changed to a high state for a predetermined period of time when the signal from the first logic family changes state; wherein:

said first and second transistor pairs are connected in parallel, and said parallel connection is connected in series with said power-down control PMOS transistor and said third PMOS transistor across the power supply terminal and ground terminal ~~levels of said system~~, wherein said third PMOS transistor is connected at the power supply terminal ~~end~~, and said first and second NMOS transistors at the ground terminal ~~end~~;

the node at which the drain terminals of said transistors of said first transistor pair being connected together is also connected to the gate of said second PMOS transistor, and the node at which the drain terminals of said transistors of said second transistor pair being connected together is also connected to the gate of said first PMOS transistor; and

the gate terminal of said first NMOS transistor serves as a ~~the~~ signal input for receiving the signal from said first ~~input~~ logic family; the gate terminal of said first PMOS transistor serves as the shifted output of the shift circuit apparatus, and the power-down control signal controls the gate terminal of said power-down control PMOS transistor ~~is controlled by a power-down control signal~~ to cut off the power to said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition.

9. (Original) The shifter circuit apparatus of claim 8, wherein said third PMOS transistor is a constant current source.

10. (Currently Amended) A dynamic CMOS level shifter circuit apparatus in a digital electronic system for shifting a signal of a first logic family at a first higher ~~lower~~ voltage level to a second lower ~~higher~~ voltage level for a second logic family, said shifter circuit apparatus being connected between a power supply terminal and a ground terminal and comprising:

a first transistor pair comprising a first NMOS and a first PMOS transistor connected in series;

a second transistor pair comprising a second NMOS and a second PMOS transistor connected in series;

a power-down control NMOS transistor; and

means for supplying a power-down control signal to the gate of the power-down control NMOS transistor, the power-down control signal being changed to a low state for a predetermined period of time when the signal from the first logic family changes state; wherein:

said first and second transistor pairs are connected in parallel, and said parallel connection is connected in series with said power-down control NMOS transistor across the power supply terminal and ground terminal ~~levels of said system~~, wherein said control NMOS transistor is connected at the power supply terminal ~~end~~, and said first and second PMOS transistors at the ground terminal ~~end~~;

the node at which the drain terminals of said transistors of said first transistor pair being connected together is also connected to the gate of said second NMOS transistor, and the node at which the drain terminals of said transistors of said second transistor pair being connected together is also connected to the gate of said first NMOS transistor; and

the gate terminal of said first PMOS transistor serves as a ~~the~~ signal input for receiving the signal from said first ~~input~~ logic family; the gate terminal of said first NMOS transistor serves as the shifted output of said shifter circuit apparatus; and the power-down control signal controls the gate terminal of said power-down control NMOS transistor ~~is controlled by a power-down control signal~~ to cut off the power to said first and second NMOS transistors for a duration of time sufficient for said first and second PMOS transistors to settle state transition.

11. (New) A level shifter coupled to a power terminal, comprising:

a level shift unit including an input terminal and an output terminal for level shifting a first voltage level to a second voltage level; and

a first transistor coupled to the level shift unit for controlling a connection between the level shift unit and the power terminal;

wherein the first transistor cuts off the connection between the level shift unit and the power terminal when the voltage level of the input terminal of the level shift unit changes, then the first transistor recovers the connection between the level shift unit and the power terminal to allow the voltage level of the output terminal of the level shift unit to change.

12. (New) The level shifter of claim 11, further comprising a second transistor, wherein the second transistor turns on to connect the output terminal of the level shift unit to a predetermined voltage terminal when the first transistor turns off.

13. (New) The level shifter of claim 11, further comprising a resistor, wherein the resistor connects the output terminal of the level shift unit and a predetermined voltage terminal.

14. (New) The level shifter of claim 11, further comprising a second transistor connected between the first transistor and the power terminal as a current source.

15. (New) The level shifter of claim 11, wherein the voltage level rating of the power terminal is selected from a group of positive-voltage rating and negative-voltage rating.

16. (New) The level shifter of claim 11, wherein the level shift unit is a level-up shift device.

17. (New) The level shifter of claim 11, further comprising a first inverter, wherein an input of the first inverter is connected to the output terminal of the level shift unit.

18. (New) The level shifter of claim 17, further comprising a second transistor, wherein the second transistor is connected to the input of the first inverter, the second transistor turns on to connect the input of the first inverter to a predetermined voltage terminal when the first transistor turns off.

19. (New) The level shifter of claim 17, further comprising a resistor, wherein the resistor connects the input of the first inverter and a predetermined voltage terminal.

20. (New) The level shifter of claim 17, further comprising a second inverter, wherein the output of the first inverter is connected to an input of the second inverter.